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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,130	12/30/2003	Alessia Pavan	2110-99-3	3296

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EXAMINER	
MOVVA, AMAR	

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,130	PAVAN ET AL.	
	Examiner	Art Unit	
	Amar Movva	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,15-26 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-26 and 31-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

PLEASE NOTE: A new examiner, Amar Movva, has been assigned to this case. Applicant is advised to note the revised contact information in the Conclusion section of this office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5,15-20,21-26, and 31-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto '630 in view of Liu '063.

a. Regarding claims 1-5,15, and 35:

i. Tanimoto discloses a non-volatile memory cell integrated on a semiconductor substrate and comprising: a floating gate transistor including a source region and a drain region (206,207, fig. 4a-5d), a gate region (fig. 4a-5d) projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region (105, fig. 4a-5d) and a control gate region (109, fig. 4a-5d), wherein said floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer (102,106, fig. 4a-5d). The floating gate regions are covered by a another

dielectric layer (107, fig. 4a-5d) before being insulated from each other through said dielectric layer. The dielectric layer is bounded between said floating gate regions (fig. 4a-5d). A memory cell matrix formed on a semiconductor substrate comprising a plurality the non-volatile memory cells organized in rows and columns (fig. 3, 4a-5d), each cell in a given row being coupled to a corresponding word line, the cell matrix being wherein adjacent memory cells being coupled to a same word line of said memory cell matrix are insulated from each other by the dielectric layer (fig. 3, 4a-5d). The dielectric layer completely fills a space between adjacent memory cells coupled to the same word line (fig. 4a-5d). Tanimoto, however, does not expressly disclose that the dielectric layer is a low-k silicon oxide layer doped with fluorine.

ii. Liu discloses a non-volatile memory cell wherein floating gates are are separated laterally via a low-k silicon oxide doped with fluorine (48/42, fig. 8a-9b, lines 27-33, col. 6).

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Liu's low-k silicon oxide layer doped with fluorine in Tanimoto's dielectric layer.

iv. The motivation to do so would have been to reduce capacitive coupling between the respective floating gates (lines 27-33, col. 6 of Liu).

b. Regarding claims 16-24, 31-34 and 36-38;

i. Tanimoto a memory-cell structure/ memory device formed on a semiconductor substrate (101, fig. 4a-5d), the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate (fig. 3,4a-5d), each memory cell in a respective row being coupled to a corresponding word line (109, fig. 4a-5d) and each memory cell including a floating gate region (fig. 3,4a-5d), the memory-cell structure including an insulating region (102,106, fig. 4a-5d) formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line. Another dielectric layer (107, fig. 4a-5d) formed on the floating gate regions. Each memory cell further comprises a control gate (109, fig. 4a-5d) region capacitively coupled to the floating gate region through another dielectric layer, and wherein the control gate regions of memory cells in respective rows are electrically interconnected (fig. 4a-5d). Each memory cell comprises a FLASH memory cell (fig. 4a-5d) in the FLASH memory device. Tanimoto, however, does not expressly disclose that the dielectric layer is a low-k silicon oxide layer doped with fluorine.

ii. Liu discloses a non-volatile memory cell wherein floating gates are are separated laterally via a low-k silicon oxide doped with fluorine (48/42, fig. 8a-9b, lines 27-33, col. 6).

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Liu's low-k silicon oxide layer doped with fluorine in Tanimoto's dielectric layer.

iv. The motivation to do so would have been to reduce capacitive coupling between the respective floating gates (lines 27-33, col. 6 of Liu).

2. Claims 1 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto '630 in view of Ahn '132.

b. Tanimoto discloses a non-volatile memory cell integrated on a semiconductor substrate and comprising: a floating gate transistor including a source region and a drain region (206,207, fig. 4a-5d), a gate region (fig. 4a-5d) projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region (105, fig. 4a-5d) and a control gate region (109, fig. 4a-5d), wherein said floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer (102,106, fig. 4a-5d). Tanimoto, however, does not expressly disclose that the dielectric layer is a low-k carbon oxide alkyl layer.

c. Ahn discloses a semiconductor device wherein the gate is insulated laterally from other gates via a low-k carbon oxide alkyl layer (140, fig. 3,[0019[0020]).

d. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Ahn's low-k carbon oxide alkyl layer in Tanimoto's dielectric layer.

e. The motivation to do so would have been to reduce capacitive coupling between the respective floating gates (lines 27-33, col. 6 of Liu).

3. Claims 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto '630/Liu '063.

a. Tanimoto/Liu discloses the device of claim 24 and that the memory device is a FLASH memory device with FLASH memory cells. Tanimoto/Liu, however, does not expressly disclose that the electronic system has a computer system.

b. It was conventional in the industry at the time of the invention to make electronic systems with memory devices placed in computer systems. Therefore it would have been obvious for the electronic system to have had a computer system in order to make use of the memory cell.

Response to Arguments

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amar Movva whose telephone number is 571-272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2891

am

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800